



Dated: 07/11/2016

A two-week ISTE STTP on CMOS, MIXED SIGNAL AND RADIO FREQUENCY VLSI DESIGN will be held at NIT MANIPUR under NME-ICT (MHRD, Govt. Of India) with the following schedules and descriptions:

**(30<sup>th</sup> January – 4<sup>th</sup> February, 2017)**

- i) Teaching faculty members from Electronics Engineering/ Electrical Engineering/ Computer Science Engineering, who are familiar with introduction to electronic circuit components, signal and system theory, VLSI design technology and basic CAD flow for electronic system are welcomed for participation.
- ii) The participants will complete the equivalent of two-week full time work online, spread over 6 physical weeks where video lectures and assignments will be uploaded beforehand.
- iii) A 6 days face to face interaction and lecture sessions will be conducted at **NIT Manipur through A-VIEW technology during 30<sup>th</sup> January – 4<sup>th</sup> February, 2017.**

For online registration please log on to: [www.nmeict.iitkgp.ernet.in/vlsidmain.php](http://www.nmeict.iitkgp.ernet.in/vlsidmain.php)

**\*\*Note:** Last date of online registration - **28<sup>th</sup> November 2016.**

- Teaching Faculty:
- a) Prof T.K. Bhattacharya, Department of ECE, IIT Kharagpur,
  - b) Prof Indrajit Chakrabarti, Department of ECE, IIT Kharagpur,
  - c) Prof Mrigank Sharad, Department of ECE, IIT Kharagpur

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